JOINT STATEMENT OF THE 26th MEETING OF THE WORLD SEMICONDUCTOR COUNCIL (WSC)

May 19th, 2022
Virtual

The world's leading semiconductor industry associations – consisting of the Semiconductor Industry Associations in China, Chinese Taipei, Europe, Japan, Korea, and the United States – held the 26th meeting of the World Semiconductor Council (WSC) today through a video conference.

The meeting was chaired by Mr. Mark Liu of TSMC and Chair of the host delegation, the Semiconductor Industry Association in Chinese Taipei. The other delegations attending the 26th WSC meeting – Semiconductor Industry Associations in China, Europe, Japan, Korea, and the United States – were chaired, respectively, by Mr. Haijun Zhao of Semiconductor Manufacturing International Corporation (SMIC), Mr. Helmut Gassel of Infineon Technologies, Mr. Takashi Miyamori of Toshiba Elec. Dev. & Storage Corp., Mr. Yong Kun Park of Skhynix, and Mr. Cristiano Amon of Qualcomm.

The WSC meets annually to bring together industry leaders to address issues of global concern to the semiconductor industry. The WSC's mandate is to encourage cooperation to promote fair competition, open trade, protection of intellectual property, technological advancement, investment liberalization, market development, and sound environmental, health and safety practices. The WSC also supports expanding the global market for information technology products and services.

Established under the "Agreement Establishing a New World Semiconductor Council" signed on June 10, 1999, and amended on May 19, 2005, the WSC has the goal of promoting cooperative global semiconductor industry activities in order to facilitate the healthy growth of the industry from a long-term global perspective. This Agreement states, "the increasing globalisation of the semiconductor industry raises important issues that must be addressed effectively through international cooperation

within the world semiconductor industry", and that "the WSC activities . . . shall be guided by principle of fairness, respect for market principles, and consistency with WTO rules and with the laws of the respective countries or regions of each Member. The WSC recognizes that it is important to ensure that markets will be open without discrimination. The competitiveness of companies and their products should be the principal determinant of industrial success and international trade."

The WSC seeks policies and regulatory frameworks that fuel innovation, propel business, and drive international competition and avoid any actions that distort markets and disrupt trade. Antitrust counsel was present throughout the meeting. During the meeting, the below reports were given and discussed, and related actions were approved.

I. Semiconductor Market Data

The WSC reviewed the semiconductor market report covering global market size, market growth, and other key industry trends. According to WSTS data, in 2021, the global semiconductor market totaled US$555.9B in revenue, up year-over-year by 26.2 percent. In terms of quantity, a total of 1,147B units of ICs were shipped in 2021, up year-over-year 20.2%.

Logic was the largest semiconductor category by sales at $154.8 billion (27.9% of 2021 total market revenue). Memory ($153.8 billion, 27.7% of 2021 total) and micro-ICs ($80.2 billion, 14.4% of 2021 total) - a category that includes microprocessors - rounded out the top three product categories in terms of total sales.

Annual country/regional sales increased in the Americas (27.3%), China (27.1%), Europe (27.5%), Japan (19.7%), and Asia Pacific/all other (25.9%). Sales by end application were led by computer (31.5%) and communication (30.7%).

While long-term growth drivers exist (AI, 5G/6G, High Performance Computing, IoT, etc.), uncertainty in the global environment may affect growth in the semiconductor market. Maintaining free and open markets globally for semiconductor products is therefore more important than ever.

II. Cooperative Approaches in Protecting the Global Environment

The WSC is firmly committed to sound and positive environmental policies and practices. The members of the WSC are proactively working together to make further progress in this area.

(1) PFC (Perfluorocompound) Emissions

The global semiconductor industry is a very minor contributor to overall emissions of greenhouse gases (GHG), and the industry is continuously working to further reduce our contribution to emissions of GHGs. One important part of our GHG emission reduction efforts is our voluntary reduction of PFC gas emissions. In 1999, the WSC (consisting at that time of each of the original regional semiconductor associations in the U.S., the European Union, Japan, Korea, and Chinese Taipei) agreed to reduce PFC emissions by at least 10% below individual baselines for each regional semiconductor association by the end of 2010. The WSC has previously announced that the industry had far surpassed this goal. Over the 10-year period, the WSC has achieved a 32% reduction. In 2011, the WSC (consisting of the five regional semiconductor associations in the 1999 agreement, with the addition of SIA in China) also announced a new voluntary PFC agreement for the next 10 years. The elements of the 2020 goal include the following:

- The implementation of best practices for new semiconductor fabs. The industry expects that the implementation of best practices will result in a Normalized Emission Rate (NER) in 2020 of 0.22 $KgCO2e/cm^2$ equivalent to a 30% NER reduction from 2010 aggregated baseline. Best practices will be continuously reviewed and updated by the WSC.
- The addition of "Rest of World" fabs (fabs located outside the WSC regions that are operated by a company from a WSC association) in reporting of emissions and the implementation of best practices for new fabs.
- A NER based measurement in kilograms of carbon equivalents per area of silicon wafers processed ($KgCO2e/cm^2$) that will be a single WSC goal at the global level.

The WSC agreed to report its progress on this new voluntary agreement on an annual basis. This external reporting will provide aggregated results of the absolute PFC consumption and emissions alongside each other and NER trends. These figures represent combined emissions for the six WSC regional associations, in their own regions and in the "Rest of World" fabs described above. In addition, to improve transparency, the WSC made its Best Practices for PFC Reduction document available on the WSC website. In 2017 the WSC has also revised its best practices document and published this update on the WSC website. The 2016 reporting also includes the reporting of newly used gases CH_2F_2, C_4F_6, C_5F_8 and C_4F_8O. In addition, the WSC reports the individual gas breakdowns.

The 2021 results will be published at the JSTC/GAMS meeting in October 2022. This revised schedule accommodates SIA in China which presently cannot collect the 2021 ESH data due to the COVID-19 situation in Shanghai.

(2) Safety and Health

The WSC is focussed on a sound proactive approach to safety and health (S&H) policies and practices, including the provision of a workplace environment that is safe and healthy for all employees.

Collecting S&H data is a typical tool which semiconductor companies use to review and manage their activities and in order to identify learnings for continuous improvement of safety and health practices. Additionally, the WSC is sharing S&H semiconductor best practices in expert settings, to advance industry practices as a whole.

Five associations have contributed to S&H aggregated data at the WSC. The 2021 results will be published at the JSTC/GAMS meeting in October 2022.

(3) Chemical Management

The WSC remains concerned about potential chemical regulatory approaches that may have a disproportionate impact on semiconductor manufacturing. **The WSC recommends that Governments/Authorities proceed carefully in regulating chemicals that are essential to the semiconductor industry. The WSC notes that**

Governments/Authorities continue to prepare new legislation for per- and polyfluoroalkyl substances (PFAS). The use of PFAS compounds remains critical for semiconductor manufacturing. The WSC recommends that Governments/Authorities take into account the limited potential risk of exposure from uses in the semiconductor industry and the chemical management practices in the semiconductor industry. The WSC recommends that any regulations provide the semiconductor industry with sufficient time to evaluate our uses of chemicals and the uses within our supply chain. If restrictions on chemicals used in our industry are deemed to be necessary and appropriate for the protection of human health and the environment, the WSC recommends that Governments/Authorities provide sufficient time for the industry to identify, qualify, and transition to alternative chemicals that satisfy our functional and performance requirements, and be provided with exemptions to allow continuation of critical uses of these chemicals in processes and articles.

III. Semiconductors: Enabling Net Zero

Semiconductors enable the transition towards a decarbonized global economy and help fight climate change by reducing society's environmental footprint. Over the past few decades, the semiconductor industry has been a leader in decreasing its climate "footprint" through voluntary greenhouse gas (GHG) emissions reduction targets in its operations, as described above in II(1) regarding PFC emissions. The industry has also increased its climate "handprint," enabling other sectors of the economy to reduce their carbon emissions and environmental impact. Further, the deployment of semiconductor-enabled technologies has empowered energy efficiency improvements, accelerated renewable energy, minimized emissions and waste, and revolutionized the way the economy functions in the digital age.

Public Sources indicate that semiconductor-enabled digital technologies can reduce greenhouse gas emissions by 15 percent, which is almost one-third of the 50 percent reduction required by 2030.[1] By making products and services "smarter," improving their efficiency, and assisting in the generation and distribution of clean

[1] See e.g. World Economic Forum, "Digital technology can cut global emissions by 15%. Here's how", 2019 (https://www.weforum.org/agenda/2019/01/why-digitalization-is-the-key-to-exponential-climate-action/)

energy, these digital technologies can further improve the greenhouse gas footprint across all sectors of the economy.

Semiconductors facilitate the ongoing shift from traditional vehicles to solutions focused on low carbon mobility, autonomous driving, and electrification. The energy savings and reduced carbon emissions from solar and wind energy and electric vehicles depend on semiconductor technology. The development of smart grids, energy management systems (EMS), and sustainable cities all rely on the Internet of Things (IoT) and information and communications technologies (ICT) driven by semiconductor advances. Energy-Efficient Ethernet reduces network power consumption by 50% or more during periods of low data traffic. Further examples of semiconductor-enabled energy efficiencies include LED lighting replacing incandescent bulbs, variable speed drives making electric motors more efficient,[2] and smart motors avoiding wasted energy in appliances, air conditioners, and industrial machinery. The digital economy also includes 3D printing that will reduce the need to transport physical goods, 5G and beyond networks that will enhance workers' ability to avoid daily commutes to the office or for medical appointments, and precision agriculture that will strengthen the food supply while reducing the use of water and pesticides.

The WSC is committed to continue pursuing technology innovations that fight climate change, advance energy efficiency, and foster sustainability. The WSC encourages GAMS to promote policies that drive adoption of semiconductor-enabled technologies as a means of improving energy efficiency and reducing GHG emissions, including recommendations set out in the United Nations Sustainable Development Goals (SDGs), which provide a roadmap to 2030 for global prosperity through action on important social and environmental issues.[3] The WSC believes semiconductor-enabled technology will continue to play a key role in realizing the SDGs by elevating

[2] World Economic Forum, "Energy efficiency is the world's 'first fuel' – and the main route to net zero, says IEA chief", 2022 (https://www.weforum.org/agenda/2022/01/iea-energy-efficiency-worlds-first-fuel-net-zero/)

[3] UN Sustainable Development Goals (https://sdgs.un.org/goals). Among many, the UN Sustainable Development Goals (SDGs) include such efforts as affordable, reliable, and sustainable energy (Goal 7); sustainable economic growth (Goal 8); resilient infrastructure and sustainable industrialization (Goal 9); inclusive and sustainable cities (Goal 11); sustainable consumption and production (Goal 12); and urgent climate action (Goal 13). The SDGs were adopted in 2015 and are built off of the UN Millennium Goals. The 2008 WSC Joint Statement endorsed Target 8F of the Millennium Goals, which aimed to expand "the benefits of new technologies, especially information and communications."
(http://www.semiconductorcouncil.org/wp-content/uploads/2016/07/08WSC-Joint-Statement-Final.pdf)

governments, businesses, civil society, and other organizations to achieve a better and more sustainable environmental future for all by 2030.

IV. Effective Protection of Intellectual Property

Standard Essential Patents

The WSC would like to highlight the increasingly important role Standard Essential Patents (SEPs) play for the semiconductor industry as one of the most innovative industrial sectors.

SEPs are patents that have been deemed necessary to implement a standard, or put in another way, the patents must be used in order to implement the standard. Almost all standards bodies require companies to license these patents using Fair, Reasonable, And Non-Discriminatory (FRAND) terms.

Recently, SEP licensing has attracted increasing attention as technological developments making use of standards have accelerated, and semiconductor devices have become ever more ubiquitous in areas such as manufacturing, transport, healthcare, and consumer electronics. The knowledge about the terms under which a given standard can be implemented is of particular relevance to the semiconductor sector.

The WSC welcomes the ongoing activities by Government/Authorities in various GAMS regions which are examining the SEP topic, including seeking inputs from stakeholders and developing guidelines.

The WSC endeavours to continue sharing information on the factors influencing SEP licensing and to provide GAMS with further information as applicable.

Patent Quality

The quality of patents is crucial to the continued growth and innovation of the semiconductor industry.

In 2018, the WSC adopted ten (10) Recommendations to Patent Offices to improve Patent Quality, along with suggested benchmarks for measuring performance on each recommended practice.

The WSC has updated the Recommendations to Patent Offices to Improve Patent Quality by emphasizing that improved patent quality results in greater certainty and predictability because fewer patents are ultimately invalidated. Defending infringement claims based on low quality patents that will be subsequently invalidated diverts resources away from research and development, thereby harming the growth of the semiconductor manufacturing industry.

In addition, the WSC has updated the recommended best practice (3) "Adequate funding" by pointing out the importance of long-term funding for Patent Offices. The WSC recommends that Governments should provide not only sufficient, but also long-term funding to Patent Offices to maintain sufficient headcount, up-to-date hardware, software and technology, and adequate training and periodic evaluation. The updated WSC Recommendations to Patent Offices to Improve Patent Quality are attached as Annex 1.

The WSC urges governments and authorities to distribute the revised WSC Recommendations to Patent Offices to Improve Patent Quality to all relevant government entities within each jurisdiction. The WSC calls on governments and authorities to support these Recommendations in the operation of their respective patent offices and to improve the quality of patents that are granted.

Abusive Patent Litigation

The WSC recognizes that abusive patent litigation seriously undermines innovation by redirecting resources to unnecessary litigation expenses and makes it more difficult for companies to bring legitimate products to market. **The WSC encourages GAMS to support the WSC Best Practices to Combat Abusive Patent Litigation.**

V. Fighting the Proliferation of Semiconductor Counterfeiting

Counterfeit semiconductor products create serious risks to the safety and health of the public and to critical national infrastructure, and can have a significant economic impact for semiconductor rights holders. Semiconductors are the "brains" inside critically important electronic systems, including healthcare and medical equipment, electric power grids, communications systems, automotive systems, and aviation systems. The WSC's Anti-Counterfeiting Task Force promotes anti-counterfeiting activities, including training and information sharing with law enforcement authorities, raising awareness, and encouraging purchases from authorized sources.

Counterfeiting threatens the innovation-driven economy that underpins prosperous societies and industry sectors like semiconductor. The WSC supports proactive industry and law enforcement activities to remove trademark infringing and counterfeit semiconductors from being offered for sale on online platforms. To promote further awareness of online challenges and mitigation practices, the WSC has produced a paper on *Counterfeit Semiconductors and the Online Environment*. The collision of the online economy and globalization has allowed criminal networks to expand the scope of their operations, free-ride on intellectual property, sell counterfeit goods directly worldwide with virtually no barriers to entry, low costs of set-up, and fewer risks of being caught. In recent years with the overall semiconductor shortage, there are indications that counterfeiters are now more active and have also shifted from large well-known B2B & B2C platforms to lesser known online platforms.

WSC members remain committed to increasing awareness of risks caused by counterfeits to the infrastructure, public health and safety. As part of WSC awareness-raising, the WSC will support the World Anti-Counterfeiting Day on June 8, 2022 which highlights the problems and risks caused by counterfeits. (See Annex 2)

The WSC has shared examples of anti-counterfeiting capacity building measures and practices that could be employed across the semiconductor industry and has circulated widely the WSC's White Paper "Winning the Battle against Counterfeit Semiconductor Products," available on the WSC website.

The WSC appreciates the GAMS' commitment to fighting semiconductor counterfeiting. The WSC looks forward to continued coordination in stopping

counterfeits and will continue to cooperate with GAMS customs and enforcement authorities across all regions of the WSC in these efforts.

The WSC recommends that GAMS members continue to implement appropriate domestic, bilateral, and multilateral IP enforcement countermeasures to deal with counterfeit semiconductors. The WSC supports GAMS coordination with their customs and law enforcement authorities to facilitate a further strengthening of IP enforcement activities at global, regional, and national levels through closer cooperation with the industry.

VI. Encryption Certification & Licensing Regulations

With the use of encryption having become widespread in commercial ICT applications, most electronic products contain semiconductors with cryptographic capabilities.

The WSC reiterates the importance of the WSC Encryption Principles, endorsed by GAMS, as they make clear that commercial encryption should not be regulated except in narrow and justifiable circumstances. Generally, there should be no regulation of cryptographic capabilities in widely available products used in the domestic commercial market because mandating or favouring specific encryption technologies will reduce, not increase, security.

In addition, based on the WSC Encryption Principles, encryption regulations should not be used for the purposes of limiting market access for foreign products. Market access, transparency, adoption of international standards, non-discriminatory and open procedures and rules for commercial encryption.

The WSC would like to highlight that compliance with the WSC Encryption Principles will help keep markets open and free from unnecessary regulation and discrimination, promote innovation, enable the dissemination of leading-edge security solutions, and thus allow the digital economy to flourish.

The WSC supports the decision by GAMS to organise an Encryption workshop in 2022, following the successful 2021 workshop.

As requested by GAMS in 2021, the WSC performed a 2022 Self-Assessment Survey of existing and draft regulatory practices, as well as issues related to commercial encryption, in relation to the WSC Encryption Principles.

The WSC encourages GAMS to continue the dialogue, making use of the results of the 2022 WSC Self-Assessment Survey to complete the review, analysis and assessment of relevant policies and measures by the 2022 GAMS Encryption Workshop and GAMS meeting with a view to the full implementation of the WSC Encryption Principles. The WSC presents a proposed agenda for the October 2022 GAMS Encryption Workshop in Annex 3.

The WSC further agrees with the *GAMS Chair's Summary* that non-discriminatory access to relevant standardization bodies, also in practice, is of utmost importance. In this context, while we appreciate that relevant contact details were provided, the WSC encourages GAMS – as per the *GAMS Chair's Summary* - to continue discussing such related topics with a bearing on encryption, including access by semiconductor companies to the TC260 Working Group 3 on Cryptography.

VII. Customs and Tariffs

Information Technology Agreement (ITA)

The ITA and its Expansion (hereinafter "the Agreement") have greatly accelerated trade in semiconductors and semiconductor-enabled technologies. The Agreement has generated a very significant increase in the value of global semiconductor-related trade, making semiconductors one of the most globally traded products today.

The large deployment of semiconductor-enabled technologies has had a profound impact on society and the economy. It has spurred productivity and made

significant contributions toward solving global societal challenges like health care, climate change, secure connectivity, education, and more.

Semiconductor technologies have also been fundamental to pandemic response as indispensable components to life-saving medical devices, and systems for public tracing and testing. They continue to play a crucial role in supporting remote healthcare and remote working and interacting solutions that will become increasingly important in our societies.

Ever faster technological innovation has continued in the semiconductor industry since the 2015 ITA-Expansion Agreement was signed. As a result, there currently are semiconductor products, manufacturing equipment, and materials which fall outside the scope of the Agreement. The rapid technological development leading to new products and emerging technologies has meant that products that were not on the market or not identified in international customs classifications at the time the Agreement was signed are now on the market but are not covered by the Agreement today. These products include a myriad of indispensable components of devices which are critical, for example, telecommunication, connectivity and transport infrastructure.

The WSC strongly supports a further ambitious tariff-elimination initiative to significantly expand product coverage of the Agreement, which has been one of the World Trade Organization (WTO)'s most successful trade deals.

Given the unique role semiconductors and semiconductor-enabled technologies play in advancing solutions to global challenges, the WSC calls on Governments and Authorities to initiate a new round of negotiations to further expand the ITA to include semiconductor-related products not previously covered. The WSC also encourages GAMS to continue to promote expansion of geographical membership of the Agreement.

Trusted Traders

The rapid and efficient international movement of goods is vital for the global semiconductor manufacturing system. Without smooth import and export processes

globally, manufacturing would become in many cases extremely difficult to realise. The semiconductor industry has been investing substantially to comply with trusted trader policies such as the Authorised Economic Operators (AEO) programs. AEO programs aim to facilitate swift import and export. Most semiconductor companies have achieved AEO status, and many of them have AEO status in multiple jurisdictions worldwide.

The WSC is grateful to GAMS for its support for enhanced cooperation with Customs authorities to improve the AEO programs to achieve harmonized and tangible trade facilitation for trusted traders. The WSC further welcomes the GAMS acknowledgment of the importance of global alignment and further mutual recognition of trusted trader programmes.

In response to the GAMS request, in 2018 the WSC articulated best practices on AEO/Trusted Traders programs. In addition, per GAMS' recommendation, on 14 April 2022 the WSC organised a separate *WSC Global AEO Workshop* with Customs agencies from the GAMS regions. A fruitful discussion took place during the workshop between WSC and Customs agencies. The WSC presented several proposals including system-based approach to controls and better coordination between AEO policies and risk management to improve the AEO programs.

Building on the successful dialogue initiated at the WSC Global AEO Workshop, the WSC would like to contribute to the further development of the *WCO SAFE Framework of Standards* to improve AEO programs. The semiconductor sector would also be well suited to participate in pilot projects, due to strong commitment to supply chain security and its general low-risk profile.

The WSC wishes to highlight that it is crucial that Customs and the industry work together to further enhance the AEO concept to future challenges.

Semiconductor-based transducers

The WSC applauds the work by World Customs Organization (WCO) to ensure the entry into force on January 1st, 2022, of the HS Explanatory Notes (HSEN) for HS heading 8541 covering semiconductor-based transducers.

However, the WSC has noticed that some of the language in the HSEN contain elements which may raise questions regarding what is covered under semiconductor-based transducers. In order to ensure clarity and avoid future potential disputes, the WSC has developed a proposal to amend the HSEN. The proposal can be found in Annex 4.

The WSC calls on GAMS to work with their Customs agencies to ensure that the WSC proposal to amend the HSEN for semiconductor-based transducers is swiftly presented at the WCO and endorsed by the contracting parties so that it will be adopted without delays.

HS Classification for semiconductors

The WSC recalls that the Harmonized System (HS) plays a fundamental role in ensuring a globally harmonised and consistent customs classification for all traded goods including semiconductors. It also creates the basis for a level playing field in international business. In case of diverging classifications of the identical semiconductor products in different jurisdictions, the WSC recommends that Customs agencies pursue clarifications at international level for harmonized and consistent classification of all semiconductor products and technologies within defined headings/subheadings.

The WSC is currently reviewing cases of diverging custom classifications for identical semiconductor products in different countries, as well as the classification of new semiconductor products and technologies, and discussing ways to address these. These cases include the issue of classification of certain semiconductor products using embedded chips/dies technology in smart PCBs. The WSC is currently discussing ways to amend the HS to classify these products. The objective is to solve the above issue via the HS Review in the WCO with support by GAMS once the WSC finalizes the

proposal. The WSC endeavours to provide more information to GAMS as soon as possible.

VIII. Regional Support Programs

Given the vital role of the semiconductor industry to all regions' economic growth and innovation, combined with the immense technological challenges and rising costs facing our industry, the WSC encourages market-based government support which fosters semiconductor industry progress and is fully consistent with the GAMS Regional Support Guidelines and Best Practices and WTO rules.

The WSC welcomes GAMS' support for full implementation of the Regional Support Guidelines and Best Practices, developed by the WSC and adopted by the GAMS in 2017. These Guidelines reflect the shared view that government support in the semiconductor sector should be transparent, non-discriminatory, and non-trade distorting; that government actions should be guided by market-based principles; and that the competitiveness of companies and their products, not the intervention of governments and authorities, should be the principal driver of innovation, industrial success and international trade.

The WSC welcomes the GAMS' ongoing commitment to increasing transparency through the regular sharing of information and analysis and assessment of subsidies and other forms of government support. Such transparency and assessment are vital to promoting consistency with the principles of the Guidelines and WTO rules, and avoiding non-market-based support that can lead to excess capacity that is not commercially justified, create unfair competitive conditions, hinder innovation, and undermine the efficiency of global value chains.

The WSC notes the responses to date on the analysis and assessment of the 30 programs originally identified in the Phase 1 Information Exchange, as well as the additional 2 programs per region in the Phase 2 Information Exchange, and recognizes the important progress to date in improving transparency and mutual understanding. The WSC notes that five programs have been identified by GAMS for further study and alignment and requests the JSTC to continue the process of information exchange to ensure comprehensive responses on both the Phase 1 and 2

programs to fully achieve the goals set out in the Regional Support Guidelines and Best Practices. The WSC continues to pursue work on the best practices for equity investments, including developing a best practice paper for equity investments.

The WSC requests GAMS to complete the analysis and assessment of these regional support programs with respect to consistency with the Regional Support Guidelines and Best Practices at a 7th Workshop on Regional Support at the 2022 GAMS Meeting. The WSC presents to GAMS a proposal for the workshop agenda, and requests that GAMS members work to finalize an agenda and invite appropriate officials in their regions to participate in this workshop (See Annex 5). The WSC also requests GAMS to continue and review the process of regular exchanges in support of full implementation of the Regional Support Guidelines and Best Practices, and continue the discussion of best practices for equity investments at the GAMS level.

The WSC welcomes the October 2021 GAMS agreement to work together to maintain the effectiveness of existing WTO disciplines, as well as to reform the WTO to help it meet new challenges.

IX. Global Supply Chain

The WSC recognizes the importance and sensitivity of global supply chain issues in the semiconductor industry. In response to GAMS' invitation to the industry to offer reflections on the global supply chain shortage that intensified during the ongoing COVID-19 global pandemic, as a first step, the WSC presents the industry's "lessons learned" on COVID-19 (see Annex 6). **The WSC urges the GAMS to continue supporting the industry's calls by prioritizing semiconductor supply chain operations as "essential business" and allowing the business travel of semiconductor workers during the ongoing COVID-19 global pandemic.**

The WSC will continue to respond to the GAMS's invitation with organized and cooperative efforts involving all associations, with endeavors to offer reflections on ways and means to increase resilience, diversity, security and transparency, including with lessons learned, that would help mitigate supply chain shortages.

X. *Responsible Minerals Sourcing*

The global semiconductor industry through the WSC is committed to using responsibly sourced' minerals in their semiconductor products. In 2018, the WSC broadened its original Conflict-Free Supply Chain Policy of 2013 to a responsible sourcing of minerals policy and referenced the deep concerns about the sources of minerals from 'conflict-affected and high-risk areas' (CAHRA).

The WSC recommends that if GAMS members are considering new responsible minerals sourcing type of legislation, that the legislation should be globally aligned to ensure that such legislation promotes the harmonization of global efforts for creating responsible supply chain management of minerals from conflict-affected and high-risk areas.

XI. *Approval of Joint Statement and Approval of Recommendations to GAMS*

The results of today's meeting will be submitted by representatives of WSC members to their respective governments/authorities for consideration at the annual meeting of WSC representatives with the Governments/Authorities Meeting on Semiconductors (GAMS) to be held in October 2022 in Japan.

XII. *Next Meeting*

The next meeting of the WSC will be hosted by the Semiconductor Industry Association in Korea in May, 2023.

XIII. *Key Documents and WSC Website:*

All key documents related to the WSC can be found on the WSC website, located at: http://www.semiconductorcouncil.org

Information on WSC member associations can be found on the following websites:

Semiconductor Industry Association in China:
http://www.csia.net.cn

Semiconductor Industry Association in Chinese Taipei:
http://www.tsia.org.tw

Semiconductor Industry Association in Europe:
http://www.eusemiconductors.eu

Semiconductor Industry Association in Japan:
http://semicon.jeita.or.jp/en/

Semiconductor Industry Association in Korea:
http://www.ksia.or.kr

Semiconductor Industry Association in the US:
http://www.semiconductors.org

Annexes:

Annex 1: Updated WSC Recommendations to Patent Offices for Improving Patent Quality
Annex 2: WSC Supports World Anti-Counterfeiting Day
Annex 3: Proposed Agenda for the October 2022 GAMS Encryption Workshop
Annex 4: Proposed Amendments to the HS Explanatory Notes for Semiconductor-Based Transducers
Annex 5: Proposed Agenda for the 7th GAMS Workshop on Regional Support
Annex 6: COVID-19: Lessons Learned for the Semiconductor Supply Chain

Annex 1

WSC Recommendations to Patent Offices for Improving Patent Quality

19 May 2022 update

The quality of patents is crucial to the continued growth and innovation of the semiconductor industry. Improved patent quality results in greater certainty and predictability because fewer patents are ultimately invalidated. Defending infringement claims based on low quality patents that will be subsequently invalidated diverts resources away from research and development, thereby harming the growth of the semiconductor manufacturing industry. The WSC recognizes the importance of improving patent quality and has been working with WIPO and the patent offices of GAMS members to encourage the collection and dissemination of standardized statistical metrics bearing on patent examination quality. Set forth below are ten recommendations from the WSC for improving patent examination quality, along with some suggested benchmarks for measuring performance on each recommended practice:

1. Examination Quality Review

Background: Even when armed with adequate technology, legal knowledge and support, there is no guarantee that an examiner's performance will be up to standard.

Recommendation: The WSC recommends that POs set up proper performance review program, with an objective measurement scale, to periodically evaluate examiners' examination quality. Poorly-performing examiners should be given support and closer supervision, and where poor performance continues should be transitioned away from examination duties.

Applicable Metrics: Actual average examination time per application (from filing until issuance as patent or abandonment) in the prior year, Average case load per examiner (Patent apps/examiner) in the prior year, Examiner turnover ratio in the prior year, Overturned internal appeals v. total internal appeals.

2. Appropriate Workload

Background: Even the best, most efficient examiners need enough time to review and examine applications, conduct prior art searches, communicate with applicants and to

do the necessary administrative work. Certain technologies may take examiners longer to review.

Recommendation: The WSC recommends that POs should determine the average time for properly examining a patent application and recruit enough examiners based on the number of annual patent applications filed within the previous year or as forecasted.

Applicable Metrics: Actual average examination time per application (from filing until issuance as patent or abandonment) in the prior year, Average number of hours allocated to examine an application.

3. Adequate Funding

Background: All factors bearing on patent quality are dependent on adequate and long-term funding. Without adequate funding, it may not be possible for POs to hire an appropriate number of examiners, to adequately train them, and arm them with the necessary resources and technology to perform at a high level. Adequate funding is therefore crucial. Yet funding needs should not impose an undue burden on applicants by way of fees such that they become an obstacle to innovation. On the other hand, fees collected from the applicants by the POs should not be used for other purposes than supporting the work of the POs

Recommendation: The WSC recommends that Governments should provide sufficient and long-term funding to POs to maintain adequate headcount, up-to-date hardware, software and technology, and adequate training and periodic evaluation. The WSC stands ready to lend its support to any PO in advocating for adequate budgets from its responsible authority.

Applicable Metrics: All metrics referenced in these Recommendations relevant to adequate funding.

4. Resources and Support

Background: Probably most important among patent quality factors is the accuracy of the patent scope (patent claims). In order to determine what the "newly invented" technology is, examiners need to find the most relevant existing technologies (the prior arts) for purposes of comparison. The internet provides access to worldwide documents, but convenience sometimes also causes trouble - too many references for the examiners to choose from. In addition, when a new application relates to cutting-

edge or highly specialized technology, examiners may have difficulty properly evaluating the value of the new invention.

Recommendation: The WSC recommends that POs should provide examiners with access to all important technology databases, in addition to patent databases. Examiners should keep a record of searched database for each case and statistics should be collected and made publicly available. POs should also consider ensuring up-to-date technology, such as the best search engine, is available for examiners to use. POs should implement an internal support system so that examiners can easily seek internal help. If appropriate, POs should also consider outsourcing all or part of the prior-art search work to reliable third party search firms. POs should use best practices in using outside experts for technology support in examination and post-grant review processes.

Applicable Metrics: Average number of database searched per case

5. Training and Qualification Requirements

Background: Examination of patent applications requires examiners to evaluate technical documents under legal standards. Technology evolves over time, as do legal standards. Examiners should be equipped with up-to-date technology and legal knowledge.

Recommendation: The WSC recommends that POs should regularly review and modify their training programs, and qualification processes for new examiners. POs should set up objective evaluation processes and standards to qualify new examiners, and only those who pass the evaluation should be allowed to examine patent applications. POs should also design and implement continuing education courses for all active examiners. Poorly-performing examiners should be given support and closer supervision, and where poor performance continues should be transitioned away from examination duties.

Applicable Metrics: Number of apps pending, Full time/part time examiner ratio in the prior year, Examiner turnover ratio in the prior year, Number of technical training hours per year/examiner.

6. Faster Administrative Procedures

Background: Although in average examiners spend only a few days to examine one patent application, it takes years for applicants to receive a formal disposition (grant, rejection). The administrative procedures, the backlog of older applications, and the

time for applicants to respond to office actions all contribute to long delays in the examination process.

Recommendation: The WSC recommends that patent offices (POs) periodically review their internal procedures and determine which steps can be simplified and/or streamlined. POs should implement a paperless environment and should encourage applicants to use an electronic filing process, whenever feasible. It is also recommended that POs should develop a strategy to clear the backlog of pending applications periodically.

Applicable Metrics: Number of apps pending at year end, Average time of first office action (from filing to first office action or search report) in the prior year, Average period of time (in months) from filing until final disposition in prior year, Actual average examination time per application (from filing until issuance as patent or abandonment), Average case load per examiner (Patent apps/examiner) in total, and average cases added annually to case load in the prior year, Average number of hours allocated to examine an application

7. Post-Grant Review Mechanism

Background: It is, of course, unrealistic to expect all patent examinations to be perfect given limited time and resources. Some patent claims will be erroneously allowed. In recognition of this, most POs have implemented a post-grant review mechanism to invalidate erroneously granted claims, but most of these mechanisms limit the evidence that challengers can adduce in the review process. For example, in some countries challengers may only present printed publications to POs during post-grant review. It is also not unheard of that some companies use post-grant review to block competitors' patents without providing threshold evidentiary support.

Recommendation: The WSC recommends that POs develop and implement robust post grant review procedures, including steps to verify the legitimacy of evidence so that challengers may present various types of evidence. POs also should conduct a threshold review of challenge requests and determine whether there is sufficient evidence to warrant initiation of a post-grant review.

Applicable Metrics: Number of patents invalidated in the prior year versus patents granted.

8. Cooperation between POs

Background: The Patent Prosecution Highway (PPH) speeds up the examination process for corresponding applications filed in cooperating POs. Through PPH, an applicant who receives a positive ruling on patent claims from one participating PO can request accelerated prosecution of corresponding claims in another participating PO. This allows applicants to obtain a patentability decision in the second office more quickly. The examiner in the office of later examination (OLE) can reuse the search and examination results from the office of earlier examination (OEE), thereby reducing workload and avoiding duplication of effort. Nonetheless, the search and examination results of a rejected application can also be very useful for the examiner in OLEs to properly examine counterpart applications.

Recommendation: The WSC recommends that POs should actively participate in PPH programs. POs should also cooperate by sharing search and examination results of all patent applications (including rejected applications), which may require mandatory disclosure of foreign counterpart applications by the applicants.

Applicable Metrics: Number of patents issued through PPH/year

9. Examination Procedures

Background: a patent application (claim) needs to meet certain legal standards – eligible subject matter, novelty, non-obviousness (inventive step) – in order to be patentable. When there are no detailed and objective guidelines on how to apply these legal standards, examiners may tend to make judgments based on their subjective viewpoint. Applicants also need to know the applicable guidelines in order to communicate efficiently with the examiners.

Recommendation: The WSC recommends that POs publish detailed, objective guidelines on how to properly determine the patentability of claims. These guidelines should provide step-by-step instructions into the examination procedures for each legal standard, and should be updated periodically to reflect current law.

Applicable Metrics: Public availability of patentability guidelines (y/n?), and published periodic updating (y/n?).

10. Transparency and Cooperation with WIPO on Patent Examination Metrics

Background: The WSC has been collaborating with WIPO and the patent offices of GAMS members to identify standardized statistical metrics bearing on patent quality and to encourage the annual collection and dissemination of such statistical information. The WSC has published a list of 12 patent quality metrics, and WIPO has

recently amended its annual IP statistical questionnaire to add a module for collecting patent examination statistics. These metrics cover workload, examination outcome, patent examiners, pendency time and post-examination opposition procedures. [See Attachment for relevant pages from the WIPO questionnaire.]

Recommendation: Mindful that the circumstances of each PO are unique, the WSC nonetheless believes that maintaining and reporting a broad array of pertinent examination-related statistics, and the comparative publication of these statistics, can serve as a useful benchmark for assessing and improving global patent examination.

The WSC urges each PO to ensure transparency of statistics related to its annual examination of patents. The WSC also urges POs to cooperate with WIPO in responding to its annual patent quality statistical questionnaire, and in periodically reviewing, augmenting and improving the statistical metrics bearing on patent examination quality. Finally, the WSC commends WIPO for coordinating this statistical initiative and encourages it to continually strive to enhance its collection of patent quality statistics.

Annex 2

8th June 2022

FOR IMMEDIATE RELEASE

WSC supports World Anti-Counterfeiting Day

On June 8th 2022, the EU's Intellectual Property Office and Global Anti-Counterfeiting Group are celebrating the 24th edition of the World Anti-Counterfeiting Day (WACD). The World Semiconductor Council (WSC) strongly supports the WACD and believes it is a great initiative to highlight the anti-counterfeit measures being taken across industries. In recent years with the overall semiconductor shortage there are indications that counterfeiters are now more active and have shifted trademark infringing online offerings of semiconductors to less well-known online platforms.

In 2012, the WSC has established an Anti-Counterfeiting Task Force amongst the semiconductor industry associations of China, Chinese Taipei, Europe, Japan, Korea, and the United States, with the aim of promoting activities to fight counterfeiting, incl. training, awareness raising, and encouraging purchases from authorised sources. The WSC works closely with governments and authorities on policies and regulations, and encourages domestic, bilateral and multilateral counter-measures and enforcement activities. Such enhanced anti-counterfeiting cooperation activities at the industry level alongside government agencies, customs and law enforcement agencies is instrumental to identify and stop parties involved in manufacturing or trafficking in counterfeit goods. The World Anti-Counterfeiting Day enables the organisation of various events focusing on particular problems of counterfeiting & piracy under the umbrella of an international outreach campaign.

According to the Organisation for Economic Co-operation and Development (OECD), international trade in counterfeit goods represented up to 2.5% of world trade, or up to USD 464 billion[4] in 2019. In view of these staggering numbers, the WSC is convinced by the importance of an initiative such as the World Anti-Counterfeiting Day, especially as counterfeit products are expected to circulate rapidly to meet current high demand, and believes it to be a great way of highlighting the common cause of fighting counterfeiting – industry sectors alongside well-informed customers, and national enforcement authorities.

About WSC

[4] Source: Organisation for Economic Co-operation and Development (OECD)–European Union Intellectual Property Office (EU IPO) (2021), *Illicit Trade, Global Trade in Fakes A WORRYING THREAT*

The World Semiconductor Council is a cooperative body of the world's leading semiconductor industry associations – consisting of the Semiconductor Industry Associations in China, Chinese Taipei, Europe, Japan, Korea and the United States – that meets annually to address issues of global concern to the semiconductor industry. The WSC also meets annually with the governments and authorities of the six regions to convey industry recommendations. The WSC is dedicated to the principle that markets should be open and competitive and works to encourage policies and regulations that fuel innovation, propel business and drive international competition in order to maintain a thriving global semiconductor industry.

More information on the WSC is available at http://www.semiconductorcouncil.org

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Annex 3

WSC Agenda Proposal for the

2022 GAMS Encryption Workshop

18 October 2022, Nagoya, Japan

09:00-9:05	Welcome and Introduction	GAMS Chair (Japan)
09:05-9:15	Report from WSC: Encryption Principles and *2022 WSC Self-Assessment Survey on Encryption*	Chair of the WSC Encryption Task Force
9:15-12:15	Continuation of the ongoing GAMS review of draft and existing policies and measures, with a view to the full implementation of the *WSC Encryption Principles* - Presentation by each GAMS delegation (5 min.) followed by - Analysis and assessment by GAMS against the *WSC Encryption Principles* • European Union • United States • China • Chinese Taipei • Japan • Korea	GAMS delegates WSC Representatives
12:15-12:30	Break	
12:30-13:00	Conclusion	GAMS Chair

Annex 4

WSC Proposed Amendments

to the Harmonised System's (HS) Explanatory Notes for Semiconductor-based Transducers, HS Heading 85.41

Legenda: ***bold italics*=** suggested amendment

~~bold italics strikethrough~~= deletions

ARTICLE 16 PROCEDURE

AMENDMENTS TO THE EXPLANATORY NOTES – HS 2022

Heading 85.41.

Page 85.41-1. Part (A).

Delete and substitute:

"**(A) SEMICONDUCTOR DEVICES (FOR EXAMPLE DIODES, TRANSISTORS, SEMICONDUCTOR BASED TRANSDUCERS)**

These are defined in Note 12 (a) (i) to this Chapter.

The operation of the devices of this group is based on the electronic properties of certain "semiconductor" materials ***(which are relevant for e.g. diodes and transistors)*** or, for the purpose of semiconductor-based transducers, on their semiconductor properties including physical (e.g., mechanical***, thermal, optical***) and chemical properties.

The main characteristics of ***these "semiconductor"*** materials is that at room temperature their resistivity lies in the range between that of conductors (metals) and that of insulators. They consist, for instance, of certain ores (e.g., crystal galena), tetravalent chemical elements (germanium, silicon, etc.) or combinations of chemical elements (e.g., trivalent and pentavalent elements, such as gallium arsenide, indium antimonide).

Semiconductor materials consisting of a tetravalent chemical element are generally monocrystalline. They are not used in their pure state but after very light doping (in a proportion expressed in parts per million) with a specific "impurity" (dopant).

For a tetravalent element, the "impurity" may be a pentavalent chemical element (phosphorus, arsenic, antimony, etc.) or a trivalent element (boron, aluminium, gallium, indium, etc.). The former

produce n-type semiconductors with excess electrons (negatively charged); the latter produce p-type semiconductors with electron deficiency, that is to say that holes (positively charged) predominate.

Semiconductor materials combining tri- and pentavalent chemical elements are also doped.

In the semiconductor materials consisting of ores, the impurities contained naturally in the ore act as dopants.

The semiconductor devices of this group generally comprise one or more "**junctions**", between p-type and n-type semiconductor materials.

They include:

(I) **Diodes** which are two-terminal devices with a single p n junction; they allow current to pass in one direction (forward) but offer a very high resistance in the other (reverse). They are used for detection, rectification, switching, etc.

The main types of diodes are signal diodes, power rectifier diodes, voltage regulator diodes, voltage reference diodes.

(II) **Transistors** are three- or four-terminal devices capable of amplification, oscillation, frequency conversion, or switching of electrical currents. The operation of a transistor depends on the variation in resistivity between two of the terminals upon the application of an electric field to the third terminal. The applied control signal or field is weaker than the resulting action brought about by the change in resistance and thus amplification results.

Transistors include:

(1) Bipolar transistors, which are three-terminal devices consisting of two diode type junctions, and whose transistor action depends on both positive and negative charge carriers (hence, bipolar).

(2) Field effect transistors (also known as metal oxide semiconductors (MOS)), which may or may not have a junction, but which depend on the induced depletion (or enhancement) of available charge carriers between two of the terminals. The transistor action in a field effect transistor employs only one type of charge carrier (hence, unipolar). A parasitic body diode, which is produced in a MOS type transistor (also known as MOSFET), may operate as a freewheeling diode during inductive load switching. MOSFET which have four terminals are known as tetrodes.

(3) Insulated Gate Bipolar Transistors (IGBT), which are three-terminal devices consisting of a gate terminal and two load terminals (emitter and collector). By applying appropriate voltages across the gate and emitter terminals, current in one direction can be controlled, i.e. turned on and turned off. IGBT chips may be incorporated with diodes in a single package (packaged IGBT devices), which protect the IGBT device and allow it to continue to function as a transistor.

(III) **Semiconductor-based transducers**

As specified in Note 12 (a) (i) to this Chapter, these are devices in which the semiconductor substrate or material plays a critical and irreplaceable role in performing their function to convert any kind of physical or chemical phenomena or an action into an electrical signal or an electrical signal into any type of physical phenomenon or an action.

The semiconductor-based transducers have the character of an independent technical unit, and can be presented either as bare die products or in a package. The components forming a semiconductor-based transducer, including active or passive discrete components indivisibly attached that enable their construction or function, must be combined to all intents and purposes indivisibly, i.e., though some of the components could theoretically be removed and replaced, this would be uneconomic under normal manufacturing conditions. Non-semiconductor-based components ~~***which do not play a key role in transducers***~~ are allowed to be part of the transducer in situations when they contribute to the transducer's function as a sensor, actuator, resonator or oscillator~~.~~***, i.e. they create conditions for the transducing semiconductor components to be protected from, or coupled to, the outside world.***

The non-semiconductor based components could protect the transducer and modify the physical or chemical quantity at the same time. The embodiment of the non-semiconductor-based component are determined by the kind of physical or chemical quantity to be transduced, e.g. light, pressure, temperature, humidity, electromagnetic radiation, electric charge etc.

Typical examples of such ***non semiconductor-based*** components are, but not limited to, the following:

(i) the package, which typically consists of metal wires for interconnection (internal or external wirebond connections), a leadframe, an encapsulation, substrates etc.; or

(ii) components which enable or support the function like magnets, optical elements etc.

The definition of the expression "semiconductor-based" also includes elements in which the semiconductor material provides functionality to the transducer by its properties, which are not only semiconductor-specific. Such properties may include mechanical strength, flexibility, thermal conductivity, optical reflectivity, chemical resistivity, etc., in combination with its ability to be manufactured with high precision on a micrometer scale by using semiconductor technology (micro machining). Such elements may include, for example membranes, bars, cantilevers, cavities, mirrors, channels, etc., which enable transducer functions by thickness or elastic flexibility).

The materials used in semiconductor-based transducers include e.g., Silicon (Si), Germanium (Ge), Carbon (C), Silicon Germanium (SiGe), Silicon Carbide (SiC), Gallium Nitride (GaN), Gallium Arsenide (GaAs), Indium Gallium Arsenide InGaAs, Gallium Phosphide (GaP), Indium Phosphide (InP), Tin Telluride (SnTe), Zinc Oxide (ZnO) and Gallium Oxide (Ga2O3).

The expression "manufactured by semiconductor technology" means the application of area processing on a wafer level that may include grinding, polishing, doping, spin coating, imaging, CVD, PVD, galvanic, developing, stripping, etching, baking, printing.

The types of semiconductor-based transducers are:

(1) Semiconductor-based sensors, which are defined in Note 12 (a) (i) (3).

One example of a sensor is a Micro-Electro-Mechanical Systems (MEMS) element used in silicon microphones as a semiconductor-based acoustic sensor. The MEMS element is made up of a stiff and perforated backplate and a flexible membrane on silicon substrate, and its function is to convert sound waves into a variable electrical output. Sound waves are physical

quantities that hit the membrane and bring it to vibration through which the varying electrical output is produced.

Another type of sensor is a gas sensor, which utilises the adsorption of electron donors/acceptors to change the resistance in graphene with an extremely high surface area.

(2) Semiconductor-based actuators, which are defined in Note 12 (a) (i) (4), e.g., electro-thermally actuated Micro-Electro-Mechanical Systems (MEMS) mirrors, which are typically used to deflect a laser beam in a broad range of applications, such as fibre-to-fibre optical switching, laser projectors, Light Detection and Ranging (LIDAR) in autonomous driving, laser tracking and position measurement, etc. Electro-thermally actuated mirrors are moved by heater elements, which act on semiconductor-based structures with different thermal expansion.

(3) **Semiconductor-based resonators,** which are defined in Note 12 (a) (i) (5), e.g., film bar acoustic wave resonators (FBAR), which are used in RF technology for multiplexing or channel selection in wireless devices.

(4) **Semiconductor-based oscillators**, which are defined in Note 12 (a) (i) (6), converting physical phenomena (stored energy of electromagnetic fields inside a resonator) into an electrical signal (output voltage with frequency depending on tuning voltage).

(IV) Other semiconductor devices

They include:

(1) **Thyristors**, consisting of four conductivity regions in semiconducting materials (three or more p n junctions) through which a direct current passes in a predetermined direction when a control pulse initiates conductivity. They are used as controlled rectifiers, as switches or as amplifiers and function as two interlocking, complementary transistors with a common collector/base junction.

(2) **Triacs** (bi-directional triode thyristors), consisting of five conductivity regions in semiconducting materials (four p n junctions) through which an alternating current passes when a control pulse initiates conductivity.

(3) **Diacs**, consisting of three conductivity regions in semiconducting materials (two p n junctions) and used to provide the pulses required to operate a triac.

(4) **Varactors** (or variable capacitance diodes).

(5) **Field effect devices**, such as gridistors.

(6) **Gunn effect devices**.

However, this group **does not include** semiconductor devices, which differ from those described above in that their operation depends primarily on temperature, pressure, etc., such as non-linear semiconductor resistors (thermistors, varistors, magneto resistors, etc.) (**heading 85.33**).

For photosensitive devices the operation of which depends on light rays (photodiodes, etc.), see group (B).

The devices described above fall in this heading whether presented mounted, that is to say, with their terminals or leads (for example pins, leads, balls, lands, bumps or pads mounted on a carrier, e.g., a substrate or a leadframe) or packaged (components), unmounted (elements) or even in the form of undiced discs (wafers). However, natural semiconductor materials (e.g., galena) are classified in this heading only when mounted.

The semiconductor-based transducers of this group, however, do not cover silicon based sensors, actuators, resonators, oscillators and combinations thereof, containing one or more monolithic, hybrid, multi-chip or multi-component integrated circuits as defined in Note 12 (b) (iv) (3) to this Chapter (**heading 85.42**).

The heading also excludes:

(a) Chemical elements (for example, silicon and selenium) doped for use in electronics, in forms unworked as drawn, or in the form of cylinders or rods (Chapter 28), when cut in the form of discs, wafers or similar forms (**heading 38.18**).

(b) Chemical compounds such as cadmium selenide and sulphide, indium arsenide, etc., containing certain additives (e.g., germanium, iodine) generally in a proportion of a few per cent, with a view to their use in electronics, whether in the form of cylinders, rods, etc., or cut into discs, wafers or similar forms (**heading 38.18**).

(c) Crystals doped for use in electronics, in the form of discs, wafers, or similar forms, polished or not, whether or not coated with a uniform epitaxial layer, provided they have not been selectively doped or diffused to create discrete regions (**heading 38.18**).

(d) Electronic integrated circuits (**heading 85.42**).

(e) Micro-assemblies of the moulded module, micromodule or similar types, consisting of discrete, active or both active and passive, components which are combined and interconnected (generally **Chapters 84, 85 or 90**).

* * *

Annex 5

7th GAMS Workshop- Agenda for Proposal (In-person)

5 min	**Welcome and Introduction by GAMS Chair**	**JP GAMS Chair**
10 min	WSC Guidelines & Best Practices	Regional Support TF Chair
40 min	Presentations on answers to questions from GAMS, WSC and JSTC on programs required for further study and alignment: • China (Presentation, Q&A)	GAMS Delegates
10 min	Q&A	GAMS Delegates Questions also by SIAs
20 min	Update from the WSC on the Discussion on Equity Investment Best Practice	Regional Support TF Chair
10 min	Coffee Break	
2.5 h	Discussion on the Scope and Basic Guidelines of the Best Practice for Equity Investments	GAMS Delegates Experts
10 min	Conclusions	JP GAMS Chair

Annex 6

COVID-19: Lessons Learned for the Semiconductor Supply Chain

Over the past two years, and with the world still gripped by the COVID-19 pandemic, semiconductor-enabled technologies allowed society to remotely work, study, treat illness, order goods online, and stay connected. As much of the world shut down, semiconductors enabled the gears of the global economy, healthcare, and the larger society to continue spinning. The COVID-19 pandemic highlighted the importance of information and communication technologies (ICT) in supporting essential activities in a crisis. The role of an ever-widening range of digitized services, from commerce to education to healthcare, is vital in building a resilient society. At the same time, restrictions associated with pandemic response threatened the ability for semiconductor companies to operate at full capacity, jeopardizing critical supply chains in the face of a growing chip shortage. It is therefore important to recognize lessons learned from the pandemic and why the semiconductor industry and supply chain was prioritized by many governments, as well as how the industry was low-risk and contributed to slowing the spread of COVID-19.

An "Essential" Industry with "Essential" Workers

The semiconductor industry is essential and governments should ensure that facilities that produce these critical components for all sectors of society and the economy remain open and operational. Restrictions on the operations of the semiconductor industry threaten essential infrastructure and life-critical equipment, such as health care and medical devices like ventilators and portable ultrasound devices, water systems and the energy grid, transportation and communication networks, and the financial system. Many of the semiconductors used in these electronic equipment pieces perform special functions and cannot be simply replaced by another semiconductor. Even for commodity semiconductors, many have been qualified and approved for a particular piece of electronic equipment, so even replacing these chips with similar devices requires testing. Thus, because the semiconductor supply chain is highly integrated and globalized, a semiconductor supply shortage or disruption in one region may cause unpredictable consequences on downstream industries across the globe.

As the COVID-19 outbreak evolved into a global pandemic, government officials around the world imposed border closures, business-shutdowns, shelter-in-place orders, and other restrictions on business and social activity to slow the spread of the virus. The vast majority of governments with a strong semiconductor footprint recognized the semiconductor industry, its supply chain, and workers as "essential" for the purpose of the public health crisis, allowing companies to stay operational while practicing strict minimal staffing, social distancing and sanitization measures. Industry workers, such as operators, technicians, and maintenance personnel, as well as scientists and engineers, were able to maintain in-person, worksite continuity.

Many countries also preserved essential international travel that is crucial to maintain critical on-site operations with the cross-border movement of technical experts and decision-makers. For example, technicians from a semiconductor manufacturing equipment company typically must travel to semiconductor factories in other countries to install or repair specialized tools in situations that are beyond the expertise of the local field office and too complicated to handle by video conference. Similarly, at times semiconductor-based solutions, such as cloud computing, must be implemented or optimized on-site for the equipment to achieve full capacity.

Additionally, as vaccines became available for those outside of health care workers and vulnerable populations, vaccines for essential workers, including those in the semiconductor industry, were often part of the next group for distribution. This allowed for a quicker return to in-person work and continued manufacturing capacity in the chip industry for workers who cannot perform their work remotely and who are part of the global supply chains providing essential products worldwide.

Amid ongoing and emerging COVID-19 outbreaks or in future public health crises, governments around the world should recognize the essentiality of the semiconductor industry to pandemic response and economic recovery, and afford semiconductor supply chain operations and industry workers an "essential" designation.

Fabs are Low-Risk Workplaces

Semiconductor industry cleanroom operations minimize the risk of virus transmission due to higher levels of automation and the cleanroom environment on the factory floor. Cleanrooms, which can cover thousands of square meters, are specially constructed facilities where contaminants, including airborne particulates, are eliminated through specialized filtration and tight controls of air flow, air pressure, temperature and humidity. Strict rules and procedures are followed to prevent contamination. Workers that operate in cleanrooms must enter and leave through airlocks, and wear full protective clothing, including hoods, face masks, gloves, boots, and coveralls. While ambient air in a typical urban area contains 35 million particles per cubic meter in the size range of .5 micrometers, the highest-level cleanroom will have 0 particles of that size, and a maximum of only 10 particles per cubic meter in the size range of .1 micrometer. For reference, the average size of the COVID-19 microbe is .125 micrometers. These strict controls and conditions position semiconductor production facilities to be more resistant to the impact of COVID-19.

Additionally, the semiconductor industry took effective steps to protect their workers. For example, in the early stages of the pandemic, even before shelter-in-place orders, many companies suspended all travel to affected areas and restricted movement of employees between in-region facilities. Companies also reduced physical staff presence, sometimes by more than 50%, by prioritizing telework, minimizing non-essential meetings or group activities, and implementing work shifts to reduce number of staff on-site at one time.

Maximizing Worker Safety and Slowing the Spread

The semiconductor industry was willing and able to take all necessary steps to ensure workers remain healthy and safe and to assist in the effort to battle the global pandemic. Measures that many companies have taken in affected areas around the world include:

- Quarantines for employees who traveled abroad or showed cold/flu symptoms
    - Employees who have traveled to affected areas or shown symptoms are prohibited from entering company premises unless undergoing a 14-day quarantine.
- Mandatory daily health declarations
    - Employees are required to take their temperature and complete an online health declaration on a daily basis.
- Requirements for all employees to wear protective masks

    - Many companies in affected areas are requiring all employees to wear protective face masks on all company premises, including shuttles.
- A factory as a safe bubble
    - In extreme cases as governments imposed strict movement controls, governments allowed semiconductor factories to operate as a safe bubble with reduced staff working, living, and sleeping in the factory or shuttling point-to-point between the factory and a designated quarantined hotel.
- Regular sanitation and disinfection practices
    - Hand sanitizers provided at site entrances and relevant areas, and sanitation and disinfection processes carried out on a regular basis within shuttles, site lobbies, cafeterias, and other common spaces.
- Social distancing
    - Social distancing best practices are implemented on production floors, office meeting rooms, and cafeterias.
- Heightened visitor entry restrictions to company facilities worldwide
    - Some companies have restricted entry of all visitors or non-essential personnel to their facilities.
- Establishing dedicated leadership teams comprised of medical & safety experts
    - These dedicated teams work to safeguard the well-being of employees and minimize the spread of infection. They also collaborate with local governments and public health organizations.
- Vaccination requirements
    - Upon availability, many companies required employees to get vaccinated in order to limit workplace transmission and reduce the likelihood of workers getting sick.

Fighting the Pandemic with Semiconductor-enabled Technology

Semiconductors facilitated the rapid global response to the pandemic. Accurate and timely testing for COVID-19 is a vital part of assessing risk and determining treatment needs for the public, and semiconductor-enabled medical instruments advanced testing efforts. Quick temperature scans using thermal cameras or non-contact forehead infrared thermometers to prevent people with fevers from entering large buildings has been used in re-opening efforts. One semiconductor company manufactures chips for a temperature monitoring skin-patch that synchronizes with mobile devices to help assess early COVID-19 signs, and the application can be integrated with digital tracing efforts.

Furthermore, cutting-edge technologies are streamlining the research process for present-day developers in their development of vaccines and treatments. For example, one semiconductor company has developed a platform which uses natural language processing to mark-up research papers for more accurate discovery by search engines. This platform had 640 active users and over 150,000 processed scientific articles. The pandemic rapidly generated data researchers used to develop COVID-19 vaccines and treatments, and semiconductor-enabled technology allowed scientists to find the specific data they needed.

Cooperative research organizations have also maximized development capacity by leveraging economies of scale. The COVID-19 High-Performance Computing (HPC) Consortium is a cooperative network designed to join the computing capacities and data collection of groups including industry, academia, federal agencies, and international government agencies. Early in the

pandemic, a semiconductor member of this consortium deployed its AI technology to help universities, companies, and clinics lower the time required to model and run different potential treatments from weeks to minutes. This significantly saved time and resources needed to develop hypothetical solutions in wetlabs. With so many institutions using its technology, the company also created a mutually reinforcing network effect with the data generated by each client lab.